UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,209	09/12/2000	Charles W. Mitchell	1001-0135	6900

22120	7590	09/27/2004

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EXAMINER
LAU, TUNG S

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/660,209	MITCHELL ET AL.
	Examiner	Art Unit
	Tung S Lau	2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2004*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-13,15,18,20-30 and 32-37* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-13,15,18,20-30 and 32-37* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed
in the United States before the invention by the applicant for patent or (2) a patent granted on an application for
patent by another filed in the United States before the invention by the applicant for patent, except that an
international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this
subsection of an application filed in the United States only if the international application designated the United
States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 13, 20, 23, 25, 27, 30, 3, 4, 5, 7, 8, 9, 10, 11, 12, 15, 18, 21, 22, 24, 26,

28, 29, 32, 33, 34, 35, 36, 37 are rejected under 35 U.S.C. 102(e) as being

anticipated Hussain et al. (U.S. patent 6,172,611).

Regarding claim 1:

Hussain discloses an integrated circuit comprising a temperature sensor

providing a temperature measurement of the integrated circuit (Col. 1-2, Lines

57-9); a programmable storage location storing a first temperature limit value

(Col. 2-3, Lines 40-16), the programmable storage location accessible via an

instruction executed by the integrated circuit (Col. 2-3, Lines 40-16); and

compare logic coupled to the temperature sensor and the storage location to

provide an indication of a comparison between the temperature measurement

and the first temperature limit value (Col. 2-3, Lines 40-16), wherein the

integrated circuit asserts a first temperature control signal which is supplied on a

first output terminal of the integrated circuit when the temperature measurement

is above the first temperature limit value (Col. 2-3, Lines 40-16).

Regarding claim 13:

Hussain discloses a method comprising measuring a temperature of an

integrated circuit with a temperature sensor (Col. 1-2, Lines 57-9), the

temperature sensor being a circuit within the integrated circuit (Col. 1-2, Lines

57-9); comparing the measured temperature to a first limit value stored in the

integrated circuit (Col. 2-3, Lines 40-16); and generating a signal on a first output

terminal of the integrated circuit according to the comparison to control the

temperature of the integrated circuit (Col. 2-3, Lines 40-16), wherein the signal is

asserted when the measured temperature is greater than the first limit value (Col.

2-3, Lines 40-16), and wherein the signal on the first output terminal is

deasserted in response to either a control location on the integrated circuit is

being accessed or the measured temperature falling below a lower limit value,

according to a programmable mode of operation (Col. 2-3, Lines 40-16).

Regarding claim 20:

Hussain discloses a method including measuring a temperature of an integrated

circuit with a temperature sensor (Col. 1-2, Lines 57-9), the temperature sensor

being a circuit within the integrated circuit (Col. 1-2, Lines 57-9); comparing the

measured temperature to a first limit value stored in the integrated circuit;

generating a signal on a first output terminal of the integrated circuit according to

the comparison to control the temperature of the integrated circuit (Col. 2-3,

Lines 40-16); and accessing a control location in the integrated circuit to cause

the signal to be deasserted (Col. 2-3, Lines 40-16, fig. 3, unit 360).

Regarding claim 23:

Hussain discloses a method comprising measuring a temperature of an

integrated circuit with a temperature sensor (Col. 1-2, Lines 57-9), the

temperature sensor being a circuit within the integrated circuit (Col. 1-2, Lines

57-9); comparing the measured temperature to a first limit value stored in the

integrated circuit (Col. 2-3, Lines 40-16, fig. 3, unit 350); and generating a signal

on a first output terminal of the integrated circuit according to the comparison to

control the temperature of the integrated circuit (Col. 2-3, Lines 40-16, fig. 3, unit

360); comparing the measured temperature to a second limit value stored in the

integrated circuit; and asserting a second signal on a second output terminal of

the integrated circuit when the measured temperature is above the second limit

value, thereby indicating that temperature has exceeded a safe limit (Col. 2-3,

Lines 40-16, fig. 3, unit 360).

Regarding claim 25:

Hussain discloses an apparatus comprising a processor including means for

measuring a temperature of the processor and providing a measured

temperature (Col. 1-2, Lines 57-9); means for comparing the measured

temperature to at least first limit value and a second limit value (Col. 2-3, Lines

40-16); means for providing a control signal on a first output terminal of the

processor according to the comparison of the measured temperature to the first

limit value the control signal to control the temperature of the integrated circuit

(Col. 2-3, Lines 40-16, fig. 3, unit 320); and means for providing an indicator

signal on a second output terminal of the integrated circuit when the measured

temperature is above the second limit value thereby indicating that the measured

temperature has exceeded a safe limit (Col. 2-3, Lines 40-16, fig. 3, unit 355).

Regarding claim 27:

Hussain discloses a microprocessor comprising a temperature sensor providing

a temperature measurement of the integrated circuit (Col. 1-2, Lines 57-9); at

least a first and second temperature limit value stored in programmable storage

locations in the microprocessor (Col. 2-3, Lines 40-16, fig. 3, unit 315, fig. 1, unit

130), the storage locations being accessible via software executed by the

microprocessor (fig. 2, unit 230); compare logic coupled to the temperature

sensor and to the programmable storage locations storing the first and second

temperature limit values (Col. 2-3, Lines 40-16), to provide respectively a first

and second signal indicative of a comparison between the temperature

measurement and the first and second temperature limit values; and first and

second output terminals coupled to provide respectively, the first and second

signals (Col. 2-3, Lines 40-16, fig. 3, unit 350, 360).

Regarding claim 30:

Hussain discloses an integrated circuit comprising a temperature sensor to

provide a measured temperature of the integrated circuit (Col. 1-2, Lines 57-9); a

storage location to hold a first programmable value indicating a first temperature

limit (fig. 4, unit 430); and compare logic coupled to compare the measure

temperature and the first temperature limit and to provide an indication of the

comparison (fig. 3, unit 320, 350, 360), and a first output coupled to provide a

first temperature control signal corresponding to the indication provided by the

compare logic (fig. 3, unit 320, 350, 360) .

Regarding claims 3, 4, 5, 7, 8, 9, 10, 11, 12, 15, 18, 21, 22, 24, 26, 28, 29, 32, 33, 34,

35, 36, 37:

Hussain continues to disclose temperature is above limit, below the temperature

range (Col. 2-3, Lines 40-16), deasserts the signals in response to temperature

changes according to mode of operation (Col. 2-3, Lines 40-16, fig. 3, unit 355,

365), storage location is addressable accessible by instruction (fig. 4, unit 430,

440, 450, fig. 3, unit 320, 350, 360), temperature comparison is external to the IC

to asset signal (fig. 4, unit 432), contains second storage unit (fig. 2, unit 230),

third storage unit (fig. 2, unit 240)), below to a third limit value (fig. 3, unit 360)),

the IC is microprocessor (Col. 1, Lines 5-10, fig. 1, unit 130), the signal is used to

inhibit cooling device to control temperature (fig. 1, unit 152), direct control a

cooling device (fig. 1, unit 160), use sequence of instruction cause the signal to

be deasserted (fig. 3, unit 320, 350, 360), a control location in the IC, including at

least one cooling device in response to asserted signal (fig. 3, unit 320), software

accessable control register (fig. 4, unit 430), indication of the compare logic (fig.

3, unit 320, 350, 360), control temperature when excess the reference

temperature (Col. 2-3, Lines 40-16, fig. 4, unit 436, 438, 435, 437, 439),

compares to multiple temperatures (fig. 4, unit 431, 432, 435, 436, 437, 438,

439).

Claim Objections

2.   Claim 6 is objected to as being dependent upon a rejected base claim, but would

be allowable if rewritten in independent form including all the limitation of the

base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: prior art fail to

teach the temperature limit value is a panic value.

Any comments considered necessary by applicant must be submitted no later

than the payment of the issue fee and, to avoid processing delays, should

preferably accompany the issue fee. Such submissions should be clearly labeled

"Comments on Statement of Reasons for Allowance."

Response to Arguments

3.   Applicant's arguments filed 9-10-2004 with respect to the pending claims have been fully considered and are persuasive. The final action of 4-23-2004 has been withdrawn.

Applicant's arguments with respect to claims 1, 13, 20, 23, 25, 27, 30, 3, 4, 5, 7, 8, 9, 10, 11, 12, 15, 18, 21, 22, 24, 26, 28, 29, 32, 33, 34, 35, 36, 37 have been considered but are moot in view of the new ground(s) of rejection.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 703-305-3309. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 703-308-3126. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841 for regular communications and 703-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TC2800 FAX Telephone Numbers: 703-872-9306

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TL

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